We claim:

1. A multithreaded very large instruction word (VLIW) processor, comprising:

a plurality of functional units for executing a plurality of instructions from an instruction stream having a plurality of threads, said threads having a priority; and

an allocator that selects instructions from said instruction stream and forwards said instructions to said plurality of functional units, said allocator selecting said instructions based on said thread priority.

2. The multithreaded very large instruction word (VLIW) processor of claim 1, wherein said thread priority allows different threads to have different priorities.

3. The multithreaded very large instruction word (VLIW) processor of claim 1, wherein said allocator selects and forwards said instructions for execution belonging to the thread with the highest priority.

4. The multithreaded very large instruction word (VLIW) processor of claim 1, wherein said allocator selects and forwards said instructions based on said thread priority and on a resource availability.

5. A multithreaded very large instruction word (VLIW) processor, comprising:

a plurality of functional units for executing a plurality of instructions from a multithreaded instruction stream; and

an allocator that selects instructions from said instruction stream and forwards said instructions to said plurality of functional units, said allocator selecting said instructions based on resource availability.

6. The multithreaded very large instruction word (VLIW) processor of claim 5, wherein said resource availability allows said instructions to be allocated only if the resources required by the instructions are available for the next cycle.

7. The multithreaded very large instruction word (VLIW) processor of claim 5, wherein said resources comprise said functional units.

8. The multithreaded very large instruction word (VLIW) processor of claim 5, wherein said allocator selects and forwards said instructions based on said resource availability and on a priority assigned to said threads.

9. A method of processing instructions from an instruction stream having a plurality of threads in a multithreaded very large instruction word (VLIW) processor, comprising the steps of:

executing said instructions using a plurality of functional units, said threads having a priority;

selecting instructions from said instruction stream based on said thread priority; and

forwarding said selected instructions to said plurality of functional units.

10. The method of claim 9, wherein said thread priority allows different threads to have different priorities.

11. The method of claim 9, wherein said selection step selects said instructions for execution belonging to the thread with the highest priority.

12. A method of processing instructions from an instruction stream having a plurality of threads in a multithreaded very large instruction word (VLIW) processor, comprising the steps of:

executing said instructions using a plurality of functional units;

selecting instructions from said instruction stream based on resource availability; and

forwarding said selected instructions to said plurality of functional units.

13. The method of claim 12, wherein said resource availability allows said instructions to be allocated only if the resources required by the instructions are available for the next cycle.

14. The method of claim 12, wherein said resources comprise said functional units.

15. An article of manufacture for processing instructions from an instruction stream having a plurality of threads in a multithreaded very large instruction word (VLIW) processor, comprising:

a computer readable medium having computer readable program code means embodied thereon, said computer readable program code means comprising program code means for causing a computer to:

execute said instructions using a plurality of functional units, said threads having a priority;

select instructions from said instruction stream based on said thread priority; and

forward said selected instructions to said plurality of functional units.

16. An article of manufacture for processing instructions from an instruction stream having a plurality of threads in a multithreaded very large instruction word (VLIW) processor, comprising:

a computer readable medium having computer readable program code means embodied thereon, said computer readable program code means comprising program code means for causing a computer to:

execute said instructions using a plurality of functional units;

select instructions from said instruction stream based on resource availability; and

forward said selected instructions to said plurality of functional units.